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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/376,654	08/18/1999	ALAN FOLMSBEE	5437-076/P41	6747

25920 7590 11/07/2006

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ART UNIT	PAPER NUMBER
2132	

DATE MAILED: 11/07/2006

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/376,654
Filing Date: August 18, 1999
Appellant(s): FOLMSBEE, ALAN

Leonard Heyman
Reg. No. 40,418
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 02 September 2005 appealing from the Office action mailed 14 June 2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,044,483	CHEN	3-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 4 recites the limitation "the error correction key" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 1, 3, 4, 13, 17, 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Chen, U.S. Patent No. 6,044,483. Referring to claims 1, 17, Chen discloses an error correction system wherein a personal computer (Col. 6, lines 30-49) contains an error detection unit (Figure 1), which meets the limitation of a central processing unit chip, processor circuitry on said chip, a programmable error correcting circuit on said chip. The system contains several DRAM units that store check bits that are used during the error correction process (Col. 11, lines 50-52 & Figure 1), which meets the limitation of RAM on said chip storing error correcting information, said RAM being in communication with said programmable error correcting circuit. The error detection unit performs error detection and correction operations on error correction code words (Col. 5, lines 3-47). If the error correction code word contains an uncorrectable error then the instruction with the error correction code word can not be executed, however, if the error is correctable, then the instruction is executed (Figure 7), which meets the limitation of the programmable error correcting circuit receives said error correcting information and processor instructions containing errors that are not capable of being executed by said processing circuitry, said programmable error correcting circuit generates corrected processor instructions in response to said processor instructions containing errors and said error correcting information, the corrected processor instructions being capable of being executed by said processing circuitry.

Referring to claims 3, 4, Chen discloses that the computer system forces errors that will be of a type that the host computer system's error control logic is capable of detecting and correcting. For example, where the computer system includes SEC DED error correcting code, the error correction notification intentionally forces errors that are correctable using the above-mentioned code (Col. 25, lines 29-41), which meets the limitation of said error correcting information includes a key that enables selection of error correction specific to an error scheme used to generate said errors, information provided in compiled computer program data in part controls said error correction, thereby providing complementary error correction with a combination of the error correction key and the information provided in the compiled computer program data.

Referring to claim 13, Chen discloses that the error correction notification intentionally forces errors that are correctable using the above-mentioned code (Col. 25, lines 29-41), which meets the limitation of wherein instructions provided to said processor include an intentional introduction of errors which are correctable with error correction algorithms, said correction algorithms pre-selected according to the key.

Referring to claim 18, Chen discloses an error correction system wherein a personal computer (Col. 6, lines 30-49) contains an error detection unit (Figure 1. The system contains several DRAM units that store check bits that are used during the error correction process (Col. 11, lines 50-52 & Figure 1), which meets the limitation of storing error correction control information on said chip. The error detection unit performs error detection and correction operations on error correction code words (Col. 5, lines 3-47). If the error correction code word contains an uncorrectable error then the instruction with the error correction code word can not

be executed, however, if the error is correctable, then the instruction is executed (Figure 7), which meets the limitation of loading instructions of said computer program onto instruction registers on a microprocessor chip, correcting said instructions using said error correction control information, executing said instructions on said chip. The computer system forces errors that will be of a type that the host computer system's error control logic is capable of detecting and correcting, which meets the limitation of intentionally placing errors in the computer program. For example, where the computer system includes SEC DED error correcting code, the error correction notification intentionally forces errors that are correctable using the above-mentioned code (Col. 25, lines 29-41.

(10) Response to Argument

Appellant's argument with respect to Chen appear to allege that Chen does not disclose a singular processor chip with the claimed elements performing the claimed functionality. Chen does disclose that the preferred embodiment of error correction logic is a single error control mechanism that is provided to perform error detection and correction on data to be read from one or more memory chips (Col. 4, lines 30-38) and embodied on a commercially available ASIC chip included on a dual in-line memory module (DIMM) card. However, Chen discloses that a non-preferred embodiment of the single error control mechanism would be embodied within a central processing unit chip (Col. 3, lines 8-12) instead of the memory module (DIMM) card. MPEP 2123 states that:

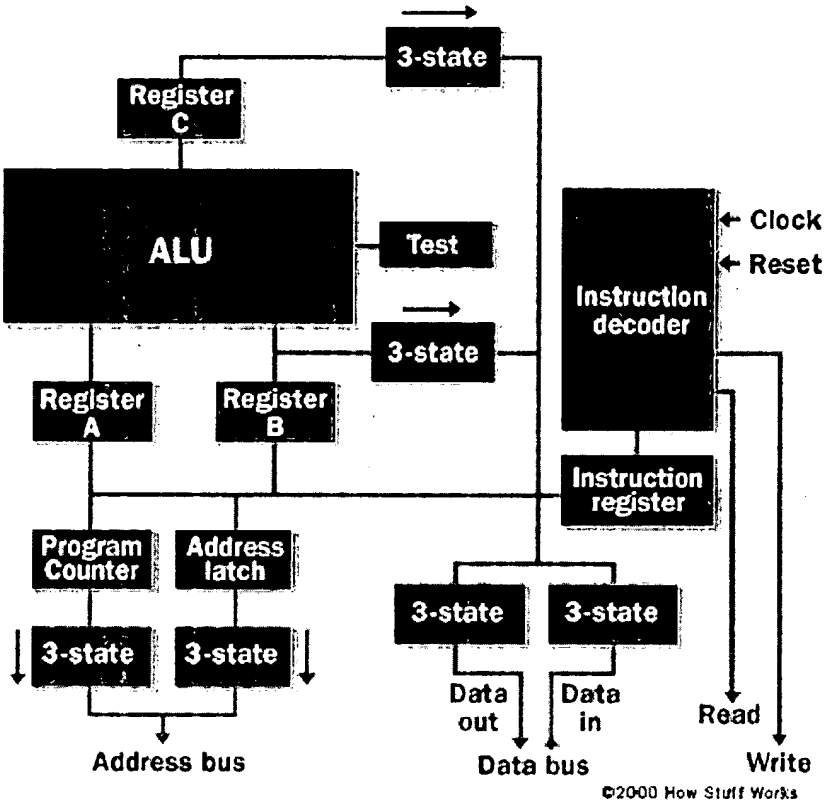
> "The use of patents as references is not limited to what the patentees describe as their own inventions or to the problems with which they are concerned. They are part of the literature of the art, relevant for all they contain." In re Heck, 699 F.2d 1331, 1332-33, 216 USPQ 1038, 1039 (Fed. Cir. 1983) (quoting In re Lemelson, 397 F.2d 1006, 1009, 158 USPQ 275, 277 (CCPA 1968)). A reference may be relied upon for all that it would have reasonably suggested to one having ordinary skill the art, including

> nonpreferred embodiments. Merck & Co. v. Biocraft Laboratories, 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989). See also Celeritas Technologies Ltd. v. Rockwell International Corp., 150 F.3d 1354, 1361, 47 USPQ2d 1516, 1522-23 (Fed. Cir. 1998) (The court held that the prior art anticipated the claims even though it taught away from the claimed invention. "The fact that a modem with a single carrier data signal is shown to be less than optimal does not vitiate the fact that it is disclosed.").
>
> and
>
> Disclosed examples and preferred embodiments do not constitute a teaching away from a broader disclosure or nonpreferred embodiments. In re Susi, 440 F.2d 442, 169 USPQ 423 (CCPA 1971). "A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." In re Gurley, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994) (The invention was directed to an epoxy impregnated fiber-reinforced printed circuit material. The applied prior art reference taught a printed circuit material similar to that of the claims but impregnated with polyester-imide resin instead of epoxy. The reference, however, disclosed that epoxy was known for this use, but that epoxy impregnated circuit boards have "relatively acceptable dimensional stability" and "some degree of flexibility," but are inferior to circuit boards impregnated with polyester-imide resins. The court upheld the rejection concluding that applicant's argument that the reference teaches away from using epoxy was insufficient to overcome the rejection since "Gurley asserted no discovery beyond what was known in the art." 27 F.3d at 554, 31 USPQ2d at 1132.). Furthermore, "[t]he prior art's mere disclosure of more than one alternative does not constitute a teaching away from any of these alternatives because such disclosure does not criticize, discredit, or otherwise discourage the solution claimed...." In re Fulton, 391 F.3d 1195, 1201, 73 USPQ2d 1141, 1146 (Fed. Cir. 2004).

Therefore, Chen discloses a singular processor chip with the claimed elements performing the claimed functionality.

It is noted that the Office Action mailed 14 June 2006 cited multiple portions of Chen in addition to Figure 7. Regardless, cited prior art references must be considered as a whole (MPEP 2141.02), and not just the cited portions.

Appellant's argument that Chen does not disclose RAM on the chip is not persuasive because Chen discloses that the central processing unit chip is a product such as the Intel Pentium Pro Microprocessor (Col. 3, lines 8-11). A simple microprocessor looks like this:



The registers in a microprocessor can be considered RAM because they are volatile data storage modules. These registers would store error correcting information when the microprocessor performs error correction (Col. 5, lines 3-24).

Appellant argues that "Chen does not mention a programmable error correcting circuit that receives error correcting information and processor instructions containing errors (claim 1, lines 9-10) wherein the error correcting information comprises a key which enables selection of error correction specific to an error correction scheme used to generate the errors." This is not persuasive because the intentionally forced errors that the host computer system error control logic is capable of detecting and correcting (Col. 25, lines 29-67) by intentionally forcing a new single bit error (Col. 25, lines 36-38), which would meet the limitation of an error correction algorithm. This intentional error forces the single bit error by inverting the logic state of a **predetermined** bit within the corrected data word (Col. 25, lines 38-41), which would meet the

limitation of the key to provide error correction. Therefore, inverting a single bit is the algorithm, and the predetermined bit is the key. The central processing unit (discussed above), would receive instructions to invert a particular predetermined bit to be capable of detecting and correcting the intentionally inserted errors as taught by Chen (Col. 25, lines 32-35).

Appellant argues, with respect to claim 17, that Chen does not teach a microprocessor. This argument is not persuasive because Chen discloses the error correction logic on a central processing unit (Col. 3, lines 8-11).

Appellant's argument that "there is no mention that the error correcting circuitry of the host computer system is programmable," is not persuasive because the error correcting logic of Chen has been programmed to detect and correct a specific type of error (i.e. inverted logic state of a predetermined bit (Col. 25, lines 35-39). The claims do not require a positive programming step. The claimed error correcting circuit from claim 17, is claimed as an element of a microprocessor, not as a process or function step of programming an error correcting circuit. Therefore, because the error correcting logic has been programmed to detect and correct a specific type of error (as mentioned above), the claim limitation is met.

Appellant's argument that the error correcting circuitry of Chen is not on the same chip as the microprocessor is not persuasive because (as mentioned above) Chen discloses that the error correction circuitry can also be implemented within a central processing unit (Col. 3, lines 8-11).

Appellant's argument that the error correcting circuitry of Chen does not select an error correction scheme based on error correction information is not persuasive because the error

correction logic of Chen contains error type indication logic that notifies the error correction logic of the type of error to be corrected (i.e. single or multiple bit errors)(Col. 26, lines 25-64).

The remainder of Appellant's arguments with respect to claim 17 have been fully addressed above.

In addition to the arguments addressed above, Appellant is arguing, with respect to claim 18, that Chen does not disclose intentionally placing errors in a computer program that is processed by the microprocessor. This argument is not persuasive because the intentionally inserted errors of Chen are inserted into read/write instructions (Col. 7, lines 1-22). Read/write instructions are a part of the operating system, which is a computer program. Therefore, Chen discloses placing errors in a computer program because the errors are inserted into read/write instructions.

Appellant's argument the Chen does not disclose executing instructions is not persuasive because Chen discloses that the read/write operations are executed (Col. 7, lines 12-18).

Once again, Appellant's arguments have failed to take into account the fact that the error correction logic described throughout the Chen reference can be implemented within a central processing unit (Col. 3, lines 8-11) as opposed to the memory module (DIMM) card, which Appellant references throughout the arguments.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Benjamin E. Lanier

Conferees:

Kim Vu KV

Kambiz Zand KAMBIZ ZAND
PRIMARY EXAMINER